Specification for 2.1″ EPD

Model NO. : GDE021A1

Prepared by	Checked by	Approved by

Customer approval

Customer	Approved by	Date of approval

smart-prototyping.com
info@smart-prototyping.com

Version	Content	Date	Producer

CONTENTS

1 General Description

GDE021A1 is an Active Matrix Electrophoretic Display(AMEPD), with interface and a reference system design. The 2.04" active area contains 172x72 pixels, and has 2-bit full display capabilities. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- 172×72 pixels display
- White reflectance above 30%
- Contrast ratio above 7:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I^2C signal master interface to read extemal temperature sensor

3 Application

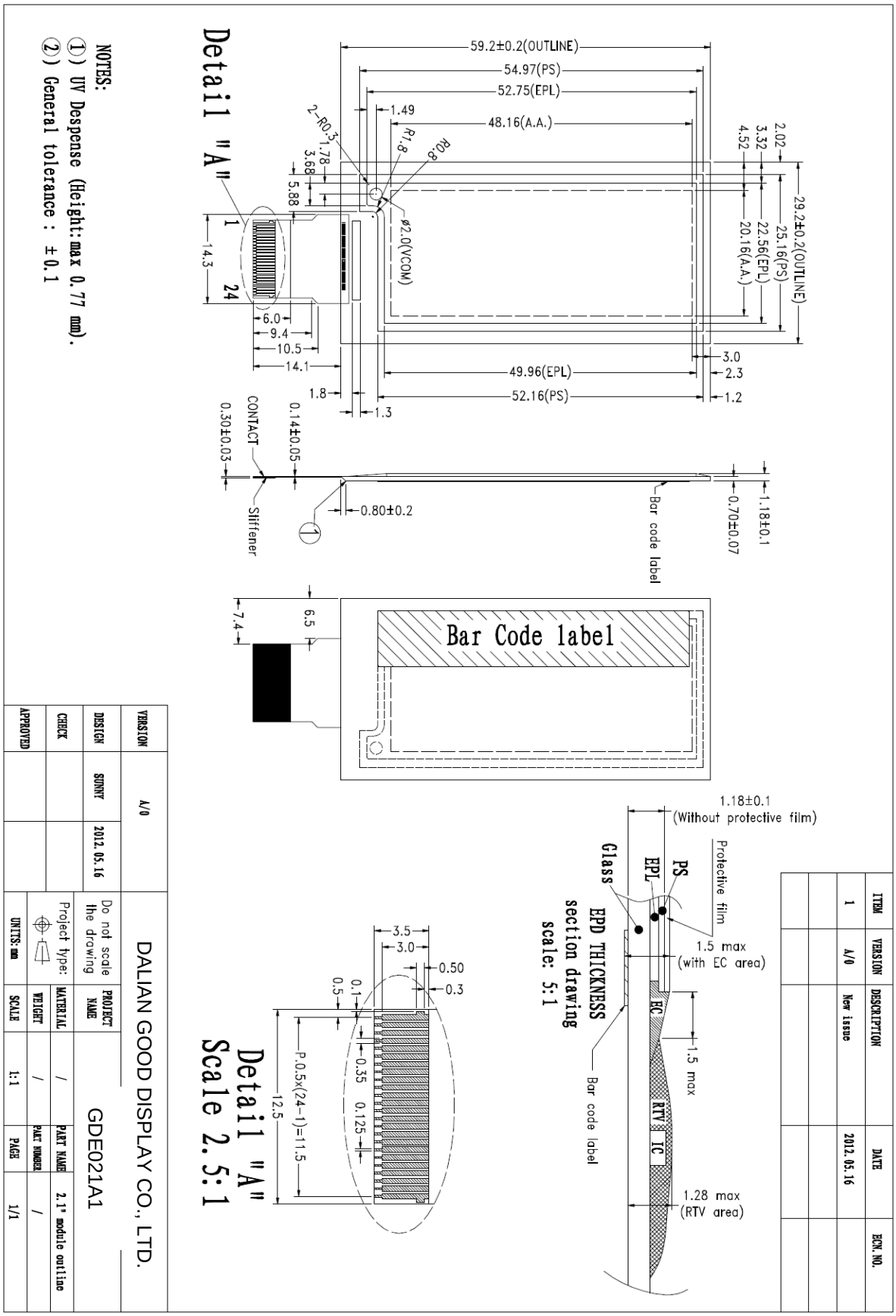
Electronic Shelf Label System

4 Mechanical Specification

4.1 Dimension

Parameter	Value	Unit	Remark
Display resolution	172×72	dots	DPI:90
Active area dimensions Width Height	 48.16 20.16	 mm mm	
Active screen size	2.04	inch	
Pixel pitch Horizontal Vertical	 0.28 0.28	 mm mm	
Pixel configuration	Rectangle		
Overall dimensions Width Height Thickness	 59.2 29.2 1.5(max.)	 mm mm mm	
Mass of the module	3.5±0.5	g	

4.2 Mechanical Drawing of EPD Module



5 Input/Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	VGL	C	Negative Gate driving voltage	
5	VGH	C	Positive Gate driving voltage	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I^2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-4
9	BUSY	O	Busy state output pin	Note 5-3
10	RES#	I	Reset signal input. Active Low.	
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	D0	I/O	Serial Clock pin (SPI)	
14	D1	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS under all circumstances	
19	VPP	C	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage	
21	PREVGH	C	Power Supply pin for VGH and VSH	
22	VSL	C	Negative Source driving voltage	
23	PREVGL	C	Power Supply pin for VCOM, VGL and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin High when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6 Driver IC Functional Block Description

6.1 On Chip Display RAM

The On chip display RAM is holding the image data. 1 set of RAM is built for historical data and the other set is built for the current image data. The size of each RAM is 128x180x2 bits. In this module, it use the RAM size of 72x172x2 bits for 72x172 resolution. The totally display data for one screen is 3096 bytes.

Shows the RAM map under the following condition:

- Command “Data Entry Mode” R11h is set to:

Address Counter update in X direction	AM=0
X: Increment Y: Increment	ID[1:0] =11

- Command “Driver Output Control” R01h is set to

180 Mux	MUX = B3h
Select G0 as 1st gate	GD = 0
Left and Right gate Interlaced	SM = 0
Scan From G0 to G179	TB = 0

- Command “Gate Start Position” R0Fh is set to:

Set the Start Position of Gate = G0	SCN=0

- Data byte sequence: DB0, DB1, DB2 … DB3095

SOURCE

X-ADDR

		S0	S1	S2	S3	S4	S5	S6	S7	…	…	S68	S69	S70	S71
		00h				01h				…		11h			
G0	00h	DB0 [7:6]	DB0 [5:4]	DB0 [3:2]	DB0 [1:0]	DB1 [7:6]	DB1 [5:4]	DB1 [3:2]	DB1 [1:0]	…	…	DB17 [7:6]	DB17 [5:4]	DB17 [3:2]	DB17 [1:0]
G1	01h	DB18 [7:6]	DB18 [5:4]	DB18 [3:2]	DB18 [1:0]	DB19 [7:6]	DB19 [5:4]	DB19 [3:2]	DB19 [1:0]	…	…	DB35 [7:6]	DB35 [5:4]	DB35 [3:2]	DB35 [1:0]
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
G170	AAh	DB3060 [7:6]	DB3060 [5:4]	DB3060 [3:2]	DB3060 [1:0]	DB3061 [7:6]	DB3061 [5:4]	DB3061 [3:2]	DB3061 [1:0]	…	…	DB3077 [7:6]	DB3077 [5:4]	DB3077 [3:2]	DB3077 [1:0]
G171	ABh	DB3078 [7:6]	DB3078 [5:4]	DB3078 [3:2]	DB3078 [1:0]	DB3079 [7:6]	DB3079 [5:4]	DB3079 [3:2]	DB3079 [1:0]	…	…	DB3095 [7:6]	DB3095 [5:4]	DB3095 [3:2]	DB3095 [1:0]

GATE

Y-ADDR

Table 6-1: RAM address map

6.2 VCOM Functional

6.2.1 VCOM Regulation

This functional block generates the voltage of VCOM, which are necessary for operating an AMEPD.

6.2.2 VCOM Sensing

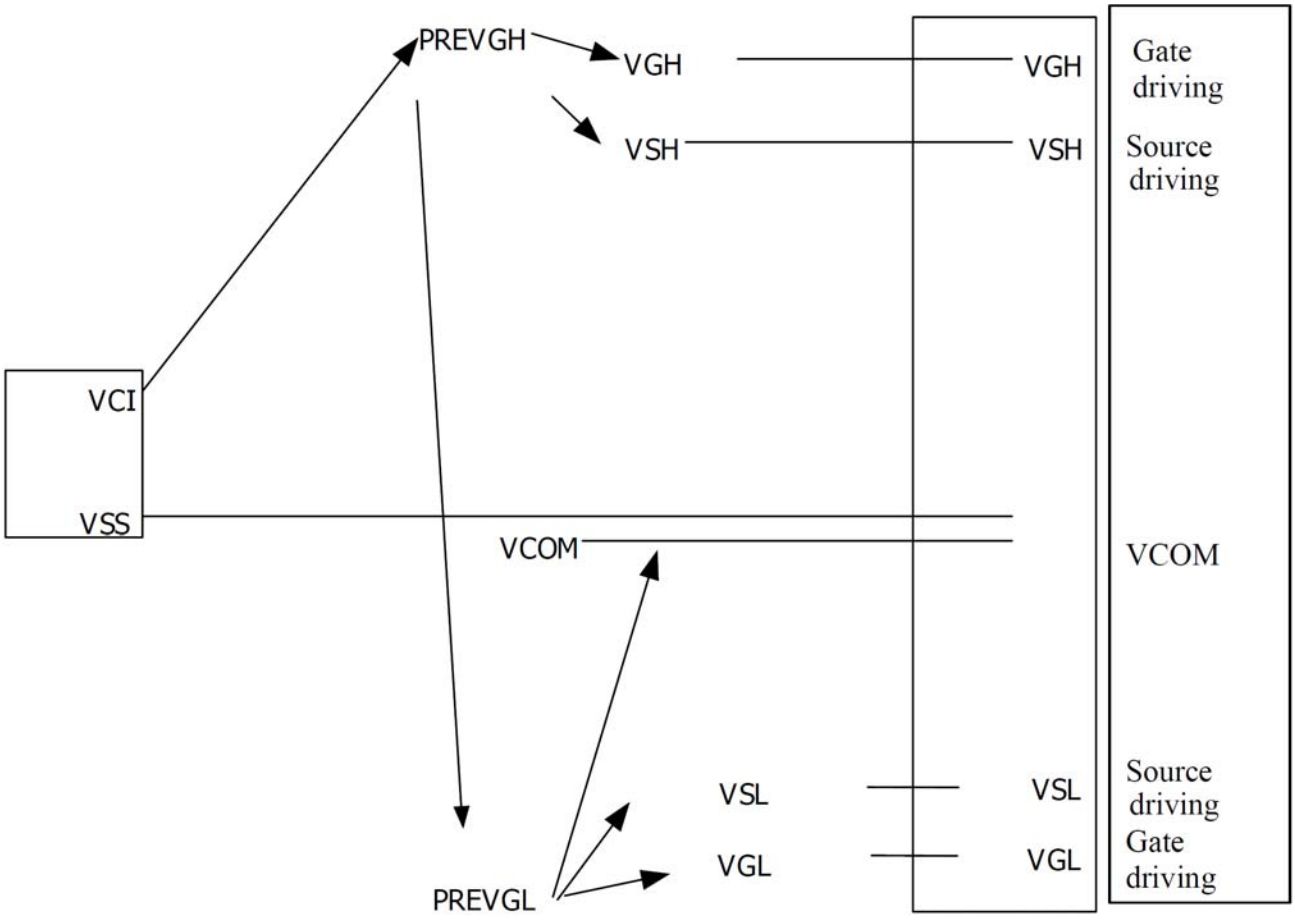
This functional block provides the scheme to select the optimal VCOM DC level and programmed the setting into OTP.

6.3 Oscillator

On-chip oscillator is included for the use on waveform timing and Booster operations.

6.4 Booster & Regulator

A voltage generation system is included in the driver. It provides all necessary driving voltage required for an AMEPD panel.



- Max voltage difference between VGH and VGL is 42V.

Figure 6-4: Input and output voltage relation chart

6.5 Waveform Look Up Table (LUT)

LUT contains 720 bits, which define the display driving waveform settings. They are arranged in following format.

In Decimal	D7	D6	D5	D4	D3	D2	D1	D0
1	VS[0-03]		VS[0-02]		VS[0-01]		VS[0-00]	
2	VS[0-13]		VS[0-12]		VS[0-11]		VS[0-10]	
3	VS[0-23]		VS[0-22]		VS[0-21]		VS[0-20]	
4	VS[0-33]		VS[0-32]		VS[0-31]		VS[0-30]	
5	VS[1-03]		VS[1-02]		VS[1-01]		VS[1-00]	
6	VS[1-13]		VS[1-12]		VS[1-11]		VS[1-10]	
7	VS[1-23]		VS[1-22]		VS[1-21]		VS[1-20]	
8	VS[1-33]		VS[1-32]		VS[1-31]		VS[1-30]	
…	…		…		…		…	
77	VS[19-03]		VS[19-02]		VS[19-01]		VS[19-00]	
78	VS[19-13]		VS[19-12]		VS[19-11]		VS[19-10]	
79	VS[19-23]		VS[19-22]		VS[19-21]		VS[19-20]	
80	VS[19-33]		VS[19-32]		VS[19-31]		VS[19-30]	
81	TP[1]				TP[0]			
82	TP[3]				TP[2]			
…	…				…			
90	TP[19]				TP[18]			

Figure 6-5: VS[n-XY] and TP[n] mapping in LUT

6.6 OTP

The OTP is the non-volatile memory and stored the information of:

- OTP Selection Option
- VCOM value
- 11 set of WAVEFORM SETTING (WS) [720bits x 11]
- 10 set of TEMPERATURE RANGE (TR) [24bits x 10]

For Programming the WS and TR, Write RAM is required, and the configurations should be:

Command: Data Entry mode	C11 D03	Set Address automatic increment setting = X increment and Y increment Set Address counter update in X direction
Command: X RAM address start /end	C44 D00 D11	Set RAM Address for S0 to S71
Command: Y RAM address start /end	C45 D00 DAB	Set RAM Address for G0 to G171
Command: RAM X address counter	C4E D00	Set RAM X AC as 0
Command: RAM Y address counter	C4F D00	Set RAM Y AC as 0

WRITE RAM ADDRESS		D7	D6	D5	D4	D3	D2	D1	D0
X	Y								
NA	NA	VCOM							
0	0	VS[0-03]				VS[0-02]			
1	0	VS[0-13]				VS[0-12]			
2	0	VS[0-23]				VS[0-22]			
3	0	VS[0-33]				VS[0-32]			
4	0	VS[1-03]				VS[1-02]			
…	…	…				…			
14	2	VS[19-23]				VS[19-22]			
15	2	VS[19-33]				VS[19-32]			
16	2	TP[1]				TP[0]			
17	2	TP[3]				TP[2]			
…	…	…				…			
25	2	TP[19]				TP[18]			
26	2	WS[1]							
…	…								
19	5								
…	…	…							
…	…								
4	28	WS[10]							
…	…								
29	30								
30	30	TEMP[1-L][7:0]							
31	30	TEMP[1-H][3:0]				TEMP[1-L][11:8]			
0	31	TEMP[1-H][11:4]							
1	31	TEMP[2-L][11:0]							
2	31								
3	31	TEMP[2-H][11:0]							
…	…	…							
…	…								
22	31	TEMP[9-L][11:0]							
23	31								
24	31	TEMP[9-H][11:0]							
25	31	TEMP[10-L][11:0]							
26	31								
27	31	TEMP[10-H][11:0]							

WS [0]

Figure 6-6: OTP Content and Address Mapping

Remark:

- WS [m] means the waveform setting of temperature set m, the configuration are same as the definition in LUT. The corresponding low temperature range of WS[m] defined as TEMP[m-L] and high range defined as TEMP [m-H]
- Load WS [m] from OTP for LUT if Temp [m-L] < Temperature Register <= Temp [m-H]

6.7 Temperature Searching Mechanism

Legend:

WS#	Waveform Setting no. #
TR#	Temperature Range no. #
LUT	720 bit register storing the waveform setting (volatile)
Temperature register	12bit Register storing reading from temperature sensor (volatile)
OTP	A non-volatile storing 11 sets of waveform setting and 10 set of temperature range
WS_sel_address	an address pointer indicating the selected WS#

OTP (non-volatile)

WS0	
WS1	TR1
WS2	TR2
WS3	TR3
WS4	TR4
WS5	TR5
WS6	TR6
WS7	TR7
WS8	TR8
WS9	TR9
WS10	TR10

Table 6-7: Waveform Setting and Temperature Range # mapping

IC implementation requirement	
1	Default selection is **WS0.**
2	Compare temperature register from **TR1 to TR10**, in sequence. **The last match will be recorded.** i.e. If the temperature register fall in both TR5 and TR7. WS7 will be selected.
3	If none of the range TR1 to TR10 is match, WS0 will be selected.
User application	
1	The default waveform should be programmed as WS0.
2	There is no restriction on the sequence of TR1, TR2….TR10.

6.8 External Temperature Sensor I^2C Single Master Interface

The chip provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing.

TSDA will treat as SDA line and TSCL will treat as SCL line. They are required connecting with external pull-up resistor.

1. If the Temperature value MSByte bit D11 = 0, then
   The temperature is positive and value (DegC) = + (Temperature value) / 16
2. If the Temperature value MSByte bit D11 = 1, then
   The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

7 Command Table

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
1	0	-	0	0	0	0	0	A_2	A_1	A_0	Status Read	Read Driver status on • A2: BUSY flag • A1,A0: Chip ID (01 as default)
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[7:0]: MUX setting as A[7:0] + 1 POR = B3h + 1 MUX B[2:0]: Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD='0', G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, … [POR] GD='1', G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0, G0, G1, G2, G3…G179 (left and right gate interlaced) [POR] SM=1, G0, G2, G4 …G178, G1, G3, …G179 B[0]: TB TB = 0, scan from G0 to G179 [POR] TB = 1, scan from G179 to G0
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	02	0	0	0	0	0	0	1	0	Reserve	
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate related driving voltage A[7:4]: VGH, 15 to 22V in 0.5V step
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
												VGH 0000 15.0 0001 15.5 0010 16.0 0011 16.5 0100 17.0 0101 17.5 0110 18.0 0111 18.5 1000 19.0 1001 19.5 1010 20.0 1011 20.5 1100 21.0 1101 21.5 1110 22.0 [POR] Others N/A A[3:0]: VGL, -15 to -20V in 0.5V step VGL default at -20V VGL 0000 -15.0 0001 -15.5 0010 -16.0 0011 -16.5 0100 -17.0 0101 -17.5 0110 -18.0 0111 -18.5 1000 -19.0 1001 -19.5 1010 -20.0 [POR] Others N/A
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source output voltage magnitude A[3:0]: VSH/VSL 10V to 17V in 0.5V step VSH/VSL 0000 10.0 0001 10.5 0010 11.0 0011 11.5 0100 12.0 0101 12.5 0110 13.0 0111 13.5 1000 14.0 1001 14.5 1010 15.0 [POR] 1011 15.5 1100 16.0 1101 16.5 1110 17.0 Others N/A
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	05	0	0	0	0	0	1	0	1	Reserve	

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	06	0	0	0	0	0	1	1	0	Reserve	
0	0	07	0	0	0	0	0	1	1	1	Display Control	Display control setting A[0]: Grey Scale (GS) mode (1bit) Mono vs 4 GS A[0] = 0: 4GS [POR] A[0] = 1: Mono In mono mode, Data 00, 01 will be treat as 0, Data 10,11 will be treat as 1 Only use transition between GS0 to GS0 or GS3 GS3 to GS0 or GS3
0	1		0	0	A_5	A_4	0	0	0	A_0		

A[4]	A[5]	Description
1	1	All Gate output voltage level as VGH
1	0	All Gate output voltage level as VGL
0	1	Selected gate output as VGL, non-selected gate output as VGH
0	0	Selected gate output as VGH, non-selected gate output as VGL [POR]

0	0	08	0	0	0	0	1	0	0	0	Reserve	
0	0	09	0	0	0	0	1	0	0	1	Reserve	
0	0	0A	0	0	0	0	1	0	1	0	Reserve	
0	0	0B	0	0	0	0	1	0	1	1	Gate and Source non overlap period Control	Set Delay of gate and source non overlap period Gate falling edge to source output change Source change to Gate rising edge Delay Duration in terms of Oscillator clock [$1/F_{OSC}$]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		

A [3:0]	Delay Duration
0000	0
0001	2
0010	4
…	
0101	10 [POR]
…	
1110	28
1111	30

0	0	0C	0	0	0	0	1	1	0	0	Reserve	
0	0	0D	0	0	0	0	1	1	0	1	Reserve	
0	0	0E	0	0	0	0	1	1	1	0	Reserve	
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start	Set the scanning start position of the

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	position	gate driver. The valid range is from 0 to 179. TB=0: SCN [7:0] = A[7:0] 00h [POR] TB=1: SCN [7:0] = 179 - A[7:0] 00h [POR]
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control
0	1		0	0	0	0	0	0	0	A_0		A[0] : Description 0 [POR] 1 Enter Deep Sleep Mode
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0]: Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2]: Set the direction in which the address counter is updated automatically after data are written to the RAM. A[2] = 0, the address counter is updated in the X direction. [POR] A[2] = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command
0	0	13	0	0	0	1	0	0	1	1	Reserve	
0	0	14	0	0	0	1	0	1	0	0	Reserve	
0	0	15	0	0	0	1	0	1	0	1	Reserve	
0	0	16	0	0	0	1	0	1	1	0	Reserve	
0	0	17	0	0	0	1	0	1	1	1	Reserve	
0	0	18	0	0	0	1	1	0	0	0	Reserve	
0	0	19	0	0	0	1	1	0	0	1	Reserve	
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	0	0	0	0		
0	0	1B	0	0	0	1	1	1	0	1	Temperature Sensor Control (Read from	Read from temperature register. X[7:0] – MSByte
1	1		X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0		

Note:If the module enter deep sleep mode, it must execute hardware RESET function to exit the deep sleep mode.

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
1	1		Y_7	Y_6	Y_5	Y_4	0	0	0	0	temperature register)	Y[7:4] – LSByte
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to temperature sensor)	Write Command to temperature sensor A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	1D	0	0	0	1	1	1	0	1	Temperature Sensor Control (Load temperature register with temperature sensor reading)	Load temperature register with temperature sensor reading BUSY=H for whole loading period The command required CLKEN=1.
0	0	1E	0	0	0	1	1	1	1	0	Reserve	
0	0	1F	0	0	0	1	1	1	1	1	Reserve	
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update	Option for Display Update

Fundamental Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>0</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>Control 1</td><td>Bypass Option used for Pattern Display, which is used for display the RAM content into the Display

OLD RAM Bypass option
A [7]
1 Enable bypass
0 Disable bypass [POR]

A[5:4] value will be used as for bypass
00 [POR]

A[3:0] Initial Update Option - Source Control

<table><tr><th></th><th>GSC A[3:2]</th><th>GSD A[1:0]</th></tr><tr><td>0000</td><td>GS0</td><td>GS0</td></tr><tr><td>0001</td><td>GS0</td><td>GS1</td></tr><tr><td>0010</td><td>GS0</td><td>GS2</td></tr><tr><td>0011 [POR]</td><td>GS0</td><td>GS3</td></tr><tr><td>0100</td><td>GS1</td><td>GS0</td></tr><tr><td>0101</td><td>GS1</td><td>GS1</td></tr><tr><td>0110</td><td>GS1</td><td>GS2</td></tr><tr><td>0111</td><td>GS1</td><td>GS3</td></tr><tr><td>1000</td><td>GS2</td><td>GS0</td></tr><tr><td>1001</td><td>GS2</td><td>GS1</td></tr><tr><td>1010</td><td>GS2</td><td>GS2</td></tr><tr><td>1011</td><td>GS2</td><td>GS3</td></tr><tr><td>1100</td><td>GS3</td><td>GS0</td></tr><tr><td>1101</td><td>GS3</td><td>GS1</td></tr><tr><td>1110</td><td>GS3</td><td>GS2</td></tr><tr><td>1111</td><td>GS3</td><td>GS3</td></tr></table></td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Display Update</td><td>Display Update Sequence Option:</td></tr>
</table>

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Control 2	Enable the stage for Master Activation Parameter (in Hex) Enable Clock Signal, Then Enable CP Then Load Temperature value Then Load LUT Then INIITIAL DISPLAY Then PATTERN DISPLAY Then Disable CP Then Disable OSC: FF [POR] Enable Clock Signal, Then Enable CP Then Load Temperature value Then Load LUT Then PATTERN DISPLAY Then Disable CP Then Disable OSC: F7 To Enable Clock Signal (CLKEN=1): 80 To Enable Clock Signal, then Enable CP (CLKEN=1, CPEN=1): C0 To INITIAL DISPLAY + PATTEN DISPLAY: 0C To INITIAL DISPLAY: 08 To DISPLAY PATTEN: 04 To Disable CP, then Disable Clock Signal (CLKEN=1, CPEN=1): 03 To Disable Clock Signal (CLKEN=1): 01 Remark: CLKEN=1: If CLS=VDDIO then Enable OSC If CLS=VSS then Enable External Clock CLKEN=0: If CLS=VDDIO then Disable OSC AND INTERNAL CLOCK Signal = VSS,
0	0	23	0	0	1	0	0	0	1	1	Reserve	
0	0	24	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.
0	0	25	0	0	1	0	0	1	0	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM, until another command is written. Address pointers will advance accordingly.
0	0	26	0	0	1	0	0	1	1	0	Reserve	
0	0	27	0	0	1	0	0	1	1	1	Reserve	

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. VCOM sense duration = Setting + 1 Seconds 0x09(10Seconds) [POR]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP
0	0	2B	0	0	1	0	1	0	1	1	Reserve	
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM register	Write VCOM register from MCU interface
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	2D	0	0	1	0	1	1	0	1	Read OTP Registers	Read register reading to MCU A [7:0] Spare OTP Option B [7:0] VCOM Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	2E	0	0	1	0	1	1	1	0	Reserve	
0	0	2F	0	0	1	0	1	1	1	1	Reserve	
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command.
0	0	31	0	0	1	1	0	0	0	1	Reserve	
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU [720 bits]
0 0 0 … 0 0	1 1 1 … 1 1		LUT [90 bytes]									
0	0	33	0	0	1	1	0	0	1	1	Read LUT register	Read from LUT register (excluding temperature data) [720 bits]
1 1 1 … 1 1	1 1 1 … 1 1		LUT [90 bytes]									
0	0	34	0	0	1	1	0	1	0	0	Reserve	
0	0	35	0	0	1	1	0	1	0	1	Reserve	
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R36h]
0	0	37	0	0	1	1	0	1	1	1	OTP selection	Write the OTP Selection:

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Control	A[7]=1 spare VCOM OTP A[6] VCOM_Status A[5]=1 spare WS OTP A[4] WS_Status A3:A0 are reserved OTP bit. User can treat the bits as Version Control.
0	0	38	0	0	1	1	1	0	0	0	Reserve	
0	0	39	0	0	1	1	1	0	0	1	Reserve	
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set number of dummy line period A[6:0]: Number of dummy line period in term of TGate 4 [POR] Available setting 0 to 127.
0	1		0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set Gate line width (TGate) A[3:0] Line width in us 0000 60 0001 64 0010 68 0011 72 0100 78 0101 84 0110 90 0111 98 1000 108 [POR] 1001 120 1010 136 1011 154 1100 180 1101 216 1110 272 1111 362 Remark: Default value will give 50Hz Frame frequency under 4 dummy line pulse setting.
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform	Select border waveform for VBD

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Control	A [7] Follow Source at Initial Update Display A [7]=0: [POR] A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE. A [6] Select GS Transition/ Fix Level for VBD A [6]=0: Select GS Transition A[3:0] for VBD A [6]=1: Select FIX level Setting A[5:4] for VBD [POR] A [5:4] Fix Level Setting for VBD 00 VSS 01 VSH 10 VSL 11[POR] HiZ A [3:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0]) 0000 GS0 GS0 0001 GS0 GS1 0010 GS0 GS2 0011 [POR] GS0 GS3 0100 GS1 GS0 0101 GS1 GS1 0110 GS1 GS2 0111 GS1 GS3 1000 GS2 GS0 1001 GS2 GS1 1010 GS2 GS2 1011 GS2 GS3 1100 GS3 GS0 1101 GS3 GS1 1110 GS3 GS2 1111 GS3 GS3
0	0	3D	0	0	1	1	1	1	0	1	Reserve	
0	0	3E	0	0	1	1	1	1	1	0	Reserve	
0	0	3F	0	0	1	1	1	1	1	1	Reserve	
0	0	40	0	1	0	0	0	0	0	0	Reserve	
0	0	41	0	1	0	0	0	0	0	1	Reserve	
0	0	42	0	1	0	0	0	0	1	0	Reserve	
0	0	43	0	1	0	0	0	0	1	1	Reserve	
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		address unit A[7:0]: XStart, POR = 00h B[7:0]: XEnd, POR = 1Fh
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[7:0]: YStart, POR = 00h B[7:0]: YEnd, POR = B3h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	46	0	1	0	0	0	1	1	0	Reserve	
0	0	47	0	1	0	0	0	1	1	1	Reserve	
0	0	48	0	1	0	0	1	0	0	0	Reserve	
0	0	49	0	1	0	0	1	0	0	1	Reserve	
0	0	4A	0	1	0	0	1	0	1	0	Reserve	
0	0	4B	0	1	0	0	1	0	1	1	Reserve	
0	0	4C	0	1	0	0	1	1	0	0	Reserve	
0	0	4D	0	1	0	0	1	1	0	1	Reserve	
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) POR is 0
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) POR is 0
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	F0	1	1	1	1	0	0	0	0	Booster Feedback Selection	Set Booster Feedback selection 0x1F = Internal Feedback is used POR is 0x1F
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1	FF	1	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

8 Command Description

8.1 Driver Output Control (01h)

This double byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		1	0	1	1	0	0	1	1
W	1						GD	SM	TB
POR							0	0	0

MUX[7:0]: Specify number of lines for the driver: MUX[7:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 180MUX.

GD: Selects the 1st output Gate

This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

SM: Change scanning order of gate driver.

When SM is set to 0, left and right interlaced is performed.

When SM is set to 1, no splitting odd / even of the GATE signal is performed, Output pin assignment sequence is shown as below (for 180 MUX ratio):

	SM=0	SM=0	SM=1	SM=1
Driver	**GD=0**	**GD=1**	**GD=0**	**GD=1**
G0	ROW0	ROW1	ROW0	ROW90
G1	ROW1	ROW0	ROW90	ROW0
G2	ROW2	ROW3	ROW1	ROW91
G3	ROW3	ROW2	ROW91	ROW1
:	:	:	:	:
G88	ROW88	ROW89	ROW44	ROW134
G89	ROW89	ROW88	ROW134	ROW44
G90	ROW90	ROW91	ROW45	ROW135
G91	ROW91	ROW90	ROW135	ROW45
:	:	:	:	:
G176	ROW176	ROW177	ROW88	ROW178
G177	ROW177	ROW176	ROW178	ROW88
G178	ROW178	ROW179	ROW89	ROW179
G179	ROW179	ROW178	ROW179	ROW89

See “Scan Mode Setting” on next page.

TB: Change scanning direction of gate driver.

This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB=0) or from bottom to up (TB=1).

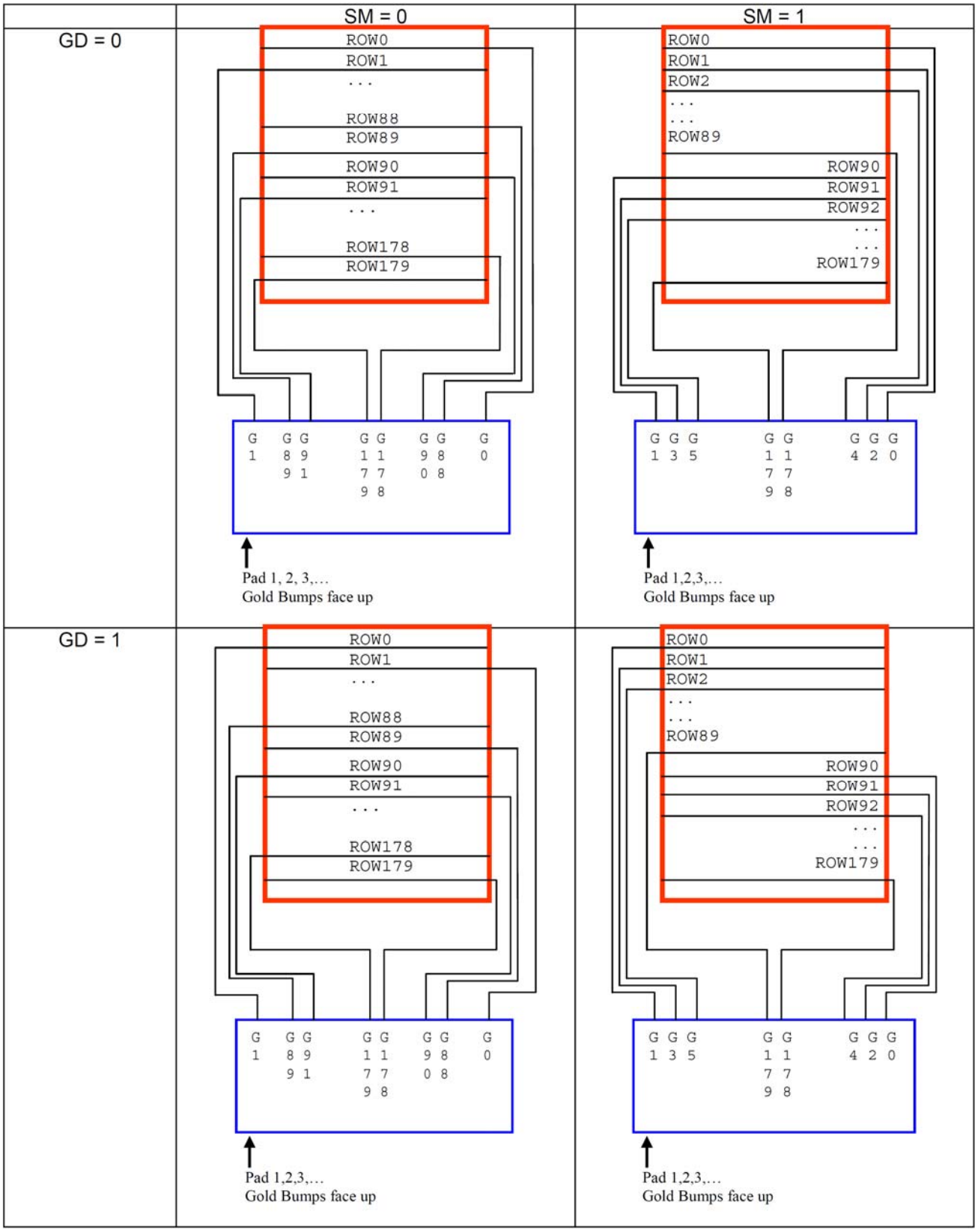


Figure 8-1: Output pin assignment on different Scan Mode Setting

8.2 Gate Scan Start Position (0Fh)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to 179. Figure 8-2 shows an example using this command of this command when MUX ratio =180 and MUX ratio = 90. "ROW" means the graphic display data RAM row.

	MUX ratio (01h) = 179	MUX ratio (01h) = 89	MUX ratio (01h) = 89
GATE Pin	Gate Start Position (0Fh) = 0	Gate Start Position (0Fh) = 0	Gate Start Position (0Fh) = 45
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
:	:	:	:
:	:	:	:
G43	:	:	-
G44	:	:	-
G45	:	:	ROW45
G46	:	:	ROW46
:	:	:	:
:	:	:	:
G88	ROW88	ROW88	:
G89	ROW89	ROW89	:
G90	ROW90	-	:
G91	ROW91	-	:
:	:	:	:
:	:	:	:
G133	:	:	ROW133
G134	:	:	ROW134
G135	:	:	-
G136	:	:	-
:	:	:	:
:	:	:	:
G176	ROW176	-	-
G177	ROW177	-	-
G178	ROW178	-	-
G179	ROW179	-	-
Display Example			

Figure 8-2: Example of Set Display Start Line with no Remapping

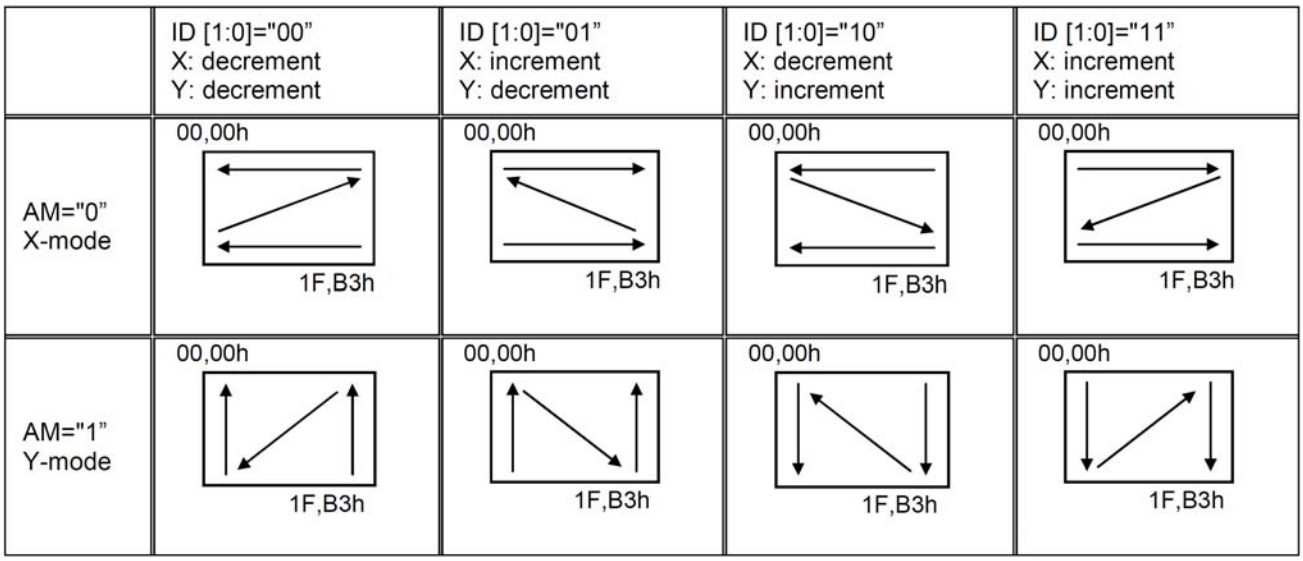
8.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

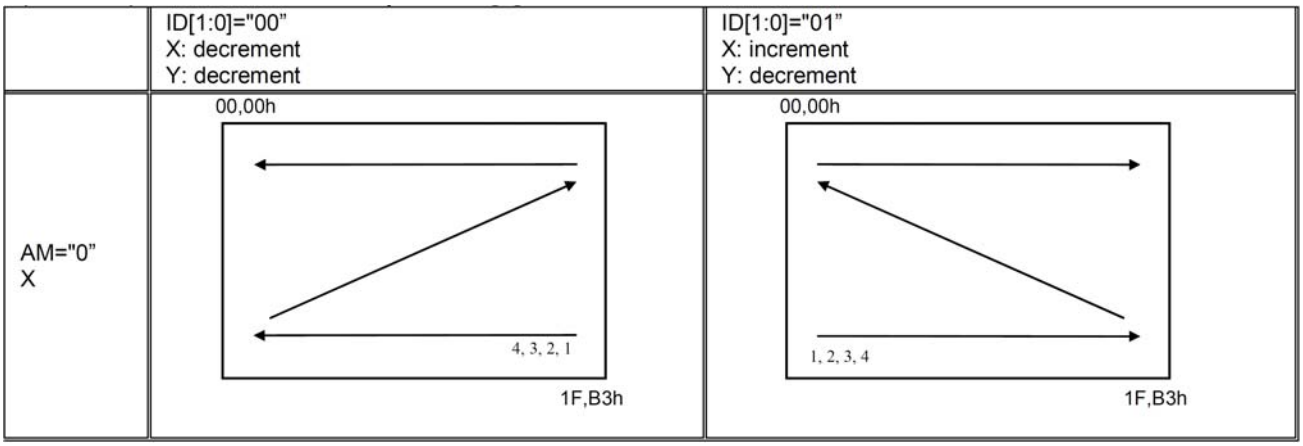
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	0	0

ID[1:0]: The address counter is automatically incremented by 1, after data are written to the RAM when ID[1:0] = "1". The address counter is automatically decremented by 1, after data are written to the RAM when ID[1:0] = "0". The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data are written to the RAM is set with AM bits.

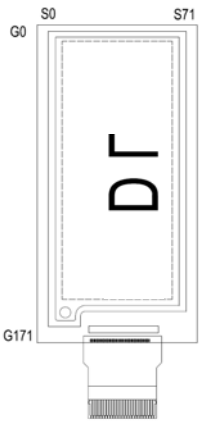
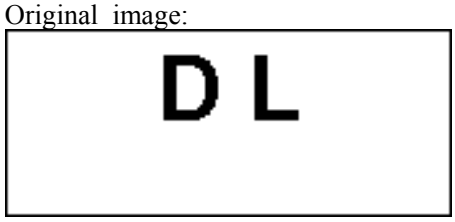
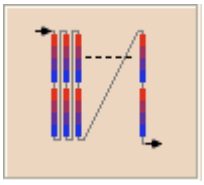
AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = "0", the address counter is updated in the X direction. When AM = "1", the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID1-0 and AM bits.



The pixel sequence are defined by the ID [0]



The totally image display style setting is shown as below table:

REG#	Style 1	Style 2	Style 3	Style 4
11h	0x03	0x02	0x01	0x00
44h	0x00	0x11	0x00	0x11
	0x11	0x00	0x11	0x00
45h	0x00	0x00	0xAB	.0xAB
	0xAB	0xAB	0x00	0x00
4Eh	0x00	0x11	0x00	0x11
4Fh	0x00	0x00	0xAB	0xAB
Image display sample				
Display data distilling format setting	1 Original image:  2 Scanning direction: vertical scan mode  3 Image display mode: Reversal display  4 The max. width :172 The max. height :72 5 Output gray: 4 gray			

8.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1				XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1				XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	0	1	1	1	1	1

XSA[4:0]/XEA[4:0]: Specify the start/end positions of the window address in the X direction by 4 times address unit. Data are written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write. It allows on XEA [4:0] ≤ XSA [4:0]. The settings follow the condition on 00h ≤ XSA [4:0], XEA [4:0] ≤ 1Fh. The windows is followed by the control setting of Data Entry Setting (R11h).

8.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		1	1	0	1	0	0	1	1

YSA[7:0]/YEA[7:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data are written to the RAM within the area determined by the addresses specified by YSA [7:0] and YEA [7:0]. These addresses must be set before the RAM write. It allows YEA [7:0] ≤ YSA [7:0]. The settings follow the condition on 00h ≤ YSA [7:0], YEA [7:0] ≤ B3h. The windows is followed by the control setting of Data Entry Setting (R11h).

8.6 Set RAM Address Counter (4Eh-4Fh)

REG#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1				XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0

XAD[4:0]: Make initial settings for the RAM X address in the address counter (AC).
YAD[7:0]: Make initial settings for the RAM Y address in the address counter (AC).

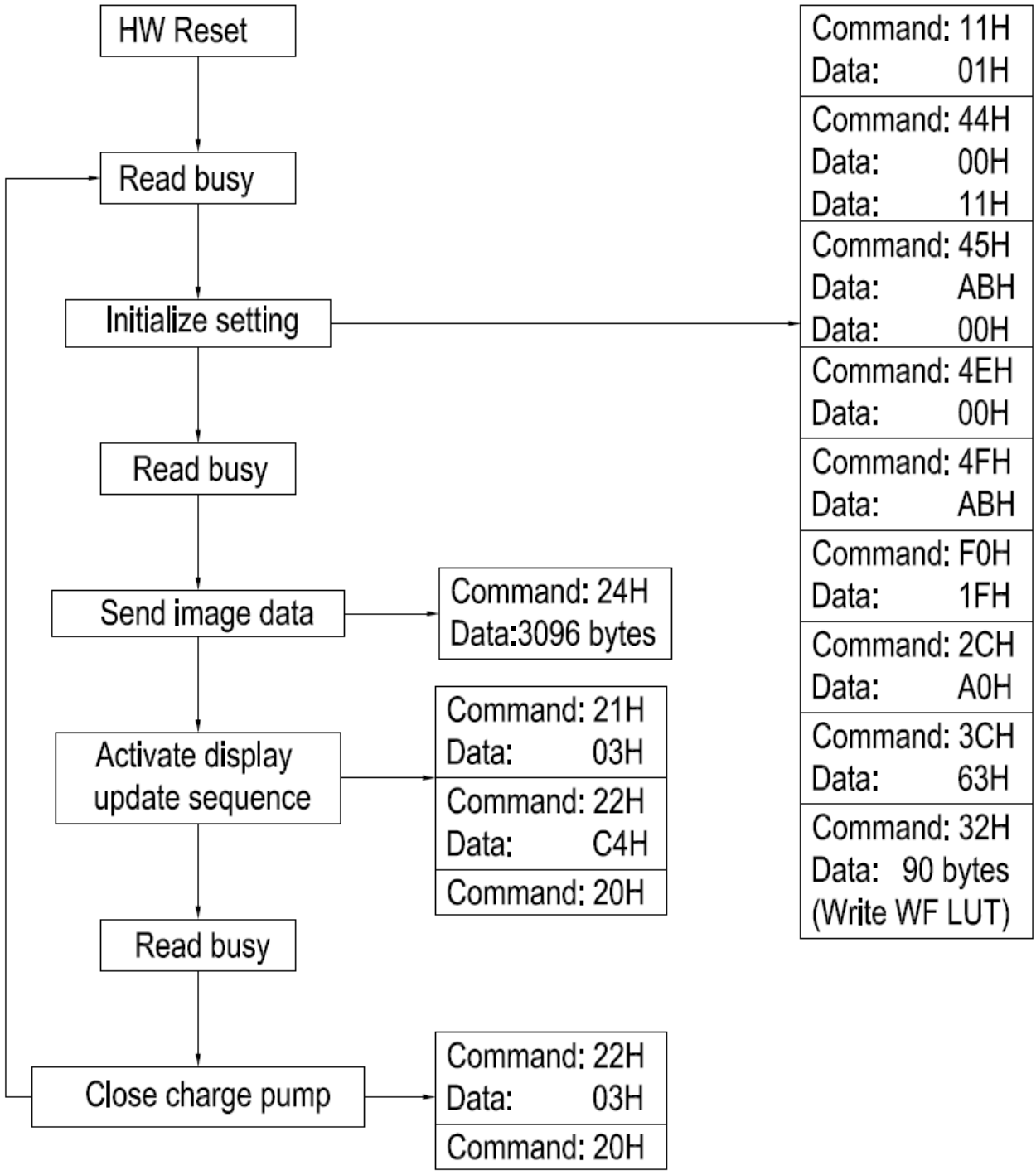
After RAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and setting for a new RAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address counter is not automatically updated when data are read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AD, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

9 Typical Operating Sequence

9.1 Normal Display

Sequence	Action by	Command	Action description	Remark
1	User	-	Power on (VCI supply)	
2	User	-	HW Reset	
	IC		After HW reset, the IC will have Registers load with POR value Ready for command input VCOM register loaded with OTP value IC enter idle mode	
3		-	Send initial code to driver including setting of	
	User	C 01	Command: Panel configuration (MUX, Source gate scanning direction)	
	User	C 03	Command: VGH / VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C 3B	Command: Set Gate line width	
	User	C 3C	Command: Select Border waveform	
4		-	Data operations	
	User	C 11	Command: Data Entry mode	
	User	C 44	Command: X RAM address start /end	
	User	C 45	Command: Y RAM address start /end	
	User	C 4E	Command: RAM X address counter	
	User	C 4F	Command: RAM Y address counter	
	User	C 24	Command: write display data to RAM	
			Ram Content for Display	
5	User	C F0 D 1F	Command: Set Internal Feedback Selection	
6	User	C 20	Command: Display update	
	IC	-	Booster and regulators turn on	
	IC	-	Load temperature register with sensor reading	
	IC	-	Load LUT register with corresponding waveform setting stored in OTP	
	IC	-	Send output waveform according initial update option	
	IC	-	Send output waveform according to data	
	IC	-	Booster and Regulators turn off	
	IC	-	Back to idle mode	
7	User	-	IC power off	

9.2 The Normal Flow Chart for Display One Screen(WF LUT Mode)



9.3 Waveform Setting OTP Program

Sequence	Action by	Command	Action description	Remark
1	User	-	Power on (VCI supply)	
2	User	-	Power on (VPP supply)	
3	User	-	HW Reset	
4	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
5	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
6	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait BUSY = L	
7	User	C 36	Program OTP selection register	
	User	-	Wait BUSY = L	
8	User	C 24	Write corresponding data into RAM	
			Following specific format	
			Write into RAM	
			Full LUT (11 entries + Temperature range) must be written at the same time	
	User	C 4E D 00 C 4F D 00	Command: Initial Ram address counter	
9	User	C 30	Waveform Setting OTP programming	
	IC	-	BUSY pin pull H	
	IC	-	Check the OTP Selection	
	IC	-	IC control OTP programming time, and transfer data to selected OTP	
	IC	-	BUSY pin pull L	
	User	-	Wait BUSY = L	
10	User	C 22 D 01 C 20	Command: CLKEN=0	
	User	-	Wait BUSY = L	
11	User		IC power off	

9.4 VCOM OTP Program

Sequence	Action by	Command	Action description	Remark
1	User	-	Power on (VCI and VPP supply)	
2	User	-	HW Reset	
3	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
4	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
5	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait until BUSY = L	
6	User	C 36	Program OTP selection register	
	User	-	Wait until BUSY = L	
	User	-	Power OFF (VPP supply)	
7		-	Send initial code to driver including setting of (or leave as POR)	VCOM sensing should have same setting during application
	User	C 01	Command: Panel configuration (MUX, Source, Gate scanning direction)	
	User	C 03	Command: VGH / VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C F0 D 1F	Command: Set Internal Feedback Selection	
	User	C 32	VCOM sense required full set of LUT for operation, USER required writing LUT in register 32h	
		-	LUT parameter	
	User	C 22 D 40 C 20	Command: Booster on and High voltage ready	
	User	-	Wait until BUSY = L	
8	User	C 28	Command: Enter VCOM sensing mode	
	IC	-	VCOM pin in sensing mode	
	IC	-	All Source cell have VSS output	
			All Gate scanning continuously	
	IC	-	Wait for 10s	According to R29h
	IC	-	Detect VCOM voltage and store in register	
	IC	-	All Gate Stop Scanning.	
	User	-	Wait until BUSY = L	

9	User	C 22 D 02 C 20	Command: Booster and High voltage disable	
	User	-	Wait until BUSY = L	
	User	-	Power On (VPP supply)	
10	User	C 2A	Command: VCOM OTP program	
	User	-	Wait until BUSY = L	
11	User	C 22 D 01 C 20	Command: CLKEN=0	
	User	-	Wait until BUSY = L	
12	User	-	IC power off (VCI and VPP Supply)	

OTP Selection bit:

Set on R37h, and read from R2Dh, A[7:6] used for VCOM and A[5:4] used for OTP

A[7:6] / [5:4]	Description
00	It indicates fresh device, OTP read and program would be made on Default OTP set. User required setting and programming the bits into 01.
01	It indicates default OTP programmed device, OTP read would be made on Default OTP set. User require setting and programming the bits into 11.
11	It indicates SPARE OTP programmed device, only OTP read would be made on SPARE OTP set. User should stop the OTP programming if 11 is found at OTP checking stage.

10 Electrical Characteristics

10.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CI}	-0.5 to +3.6	V
Logic Input voltage	V_{IN}	-0.5 to V_{CI} +0.5	V
Logic Output voltage	V_{OUT}	-0.5 to V_{CI} +0.5	V
Operation temperature range	T_{OPR}	0 to +50	°C
Storage temperature range	T_{STG}	-20 to +70	°C

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

10.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{CI}	-	VCI	2.4	3.0	3.3	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{CI}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{CI}	V
OTP Program voltage	V_{PP}	-	VPP	-	7.5	-	V
Typical power panel	P_{TYP}	-	-	-	24	36	mW
Standby power panel	P_{STPY}	-	-	-	0.006	-	mW
Typical operating current	Iopr_VCI	-	-	-	8.0	-	mA
Sleep mode current	Islp_VCI	VCI=3.3V DC/DC OFF No clock No output load Ram data retain	VCI	-	35	50	uA
Deep sleep mode current	Idslp_VCI	VCI=3.3V DC/DC OFF No clock No output load Ram data not retain	VCI	-	2	5	uA
Operation temperature range	T_{OPR}	-	-	0	-	50	°C
Storage temperature range	T_{STG}	-	-	-20	-	70	°C

Notes: 1. The typical operating current is measured with following transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Figure 10-2)
It include DC-DC circuit current with the component parameter of the typical application circuit on page 50.
2. The standby power is the consumed power when the panel controller is in standby mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OED.

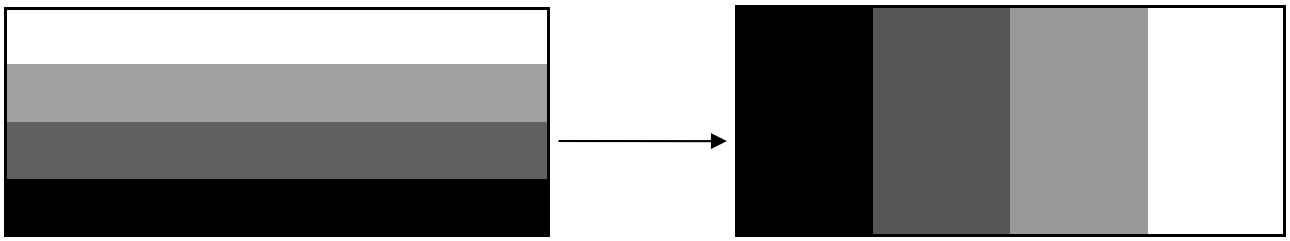


Figure 10-2 The typical power consumption measure pattern

10.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VDD operation voltage	VDD	-	VDD	1.7	1.8	1.9	V
VCOM output voltage	VCOM	-	VCOM	-4.0	-	+0.2	V
Gate output voltage	V_{GATE}	-	G0-171	-20	-	+22	V
Gate output peak to peak voltage	$V_{GATE(p-p)}$	-	G0-171	-	-	42	V
Positive Source output voltage	V_{SH}	-	S0-71	+10	-	+17	V
Negative Source output voltage	V_{SL}	-	S0-71	-	$-V_{SH}$	-	V

10.4 Panel AC Characteristics

10.4.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 10-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Connnand Interface		Control Signal		
Bus interface	**D1**	**D0**	**CS#**	**D/C#**	**RES#**
4-wire SPI	SDIN	SCLK	CS#	D/C#	RES#
3-wire SPI	SDIN	SCLK	CS#	L	RES#

Table 10-4-1: MCU interface assignment under different bus interface mode

10.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table10-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

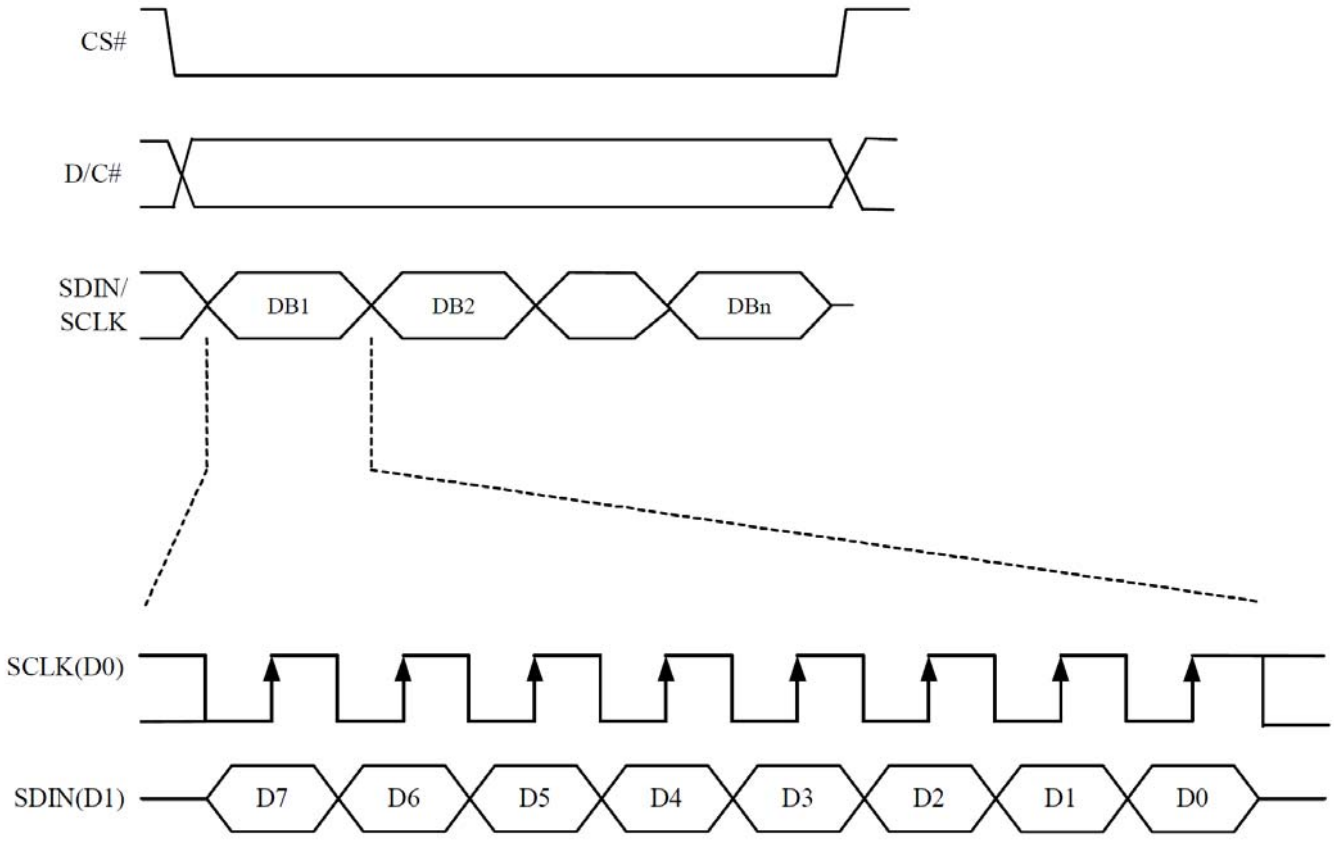


Figure 10-4-2: Write procedure in 4-wire SPI mode

10.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#. In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

Table 10-4-3: Control pins of 3-wire Serial interface

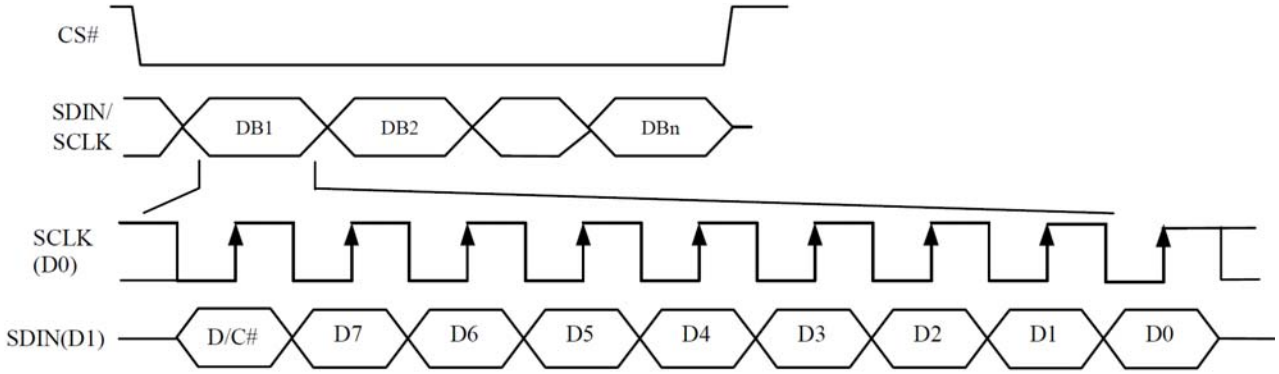


Figure 10-4-3: Write procedure in 3-wire SPI mode

10.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =25ºC.

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.4 to 3.3V	CL	0.95	1	1.05	MHz

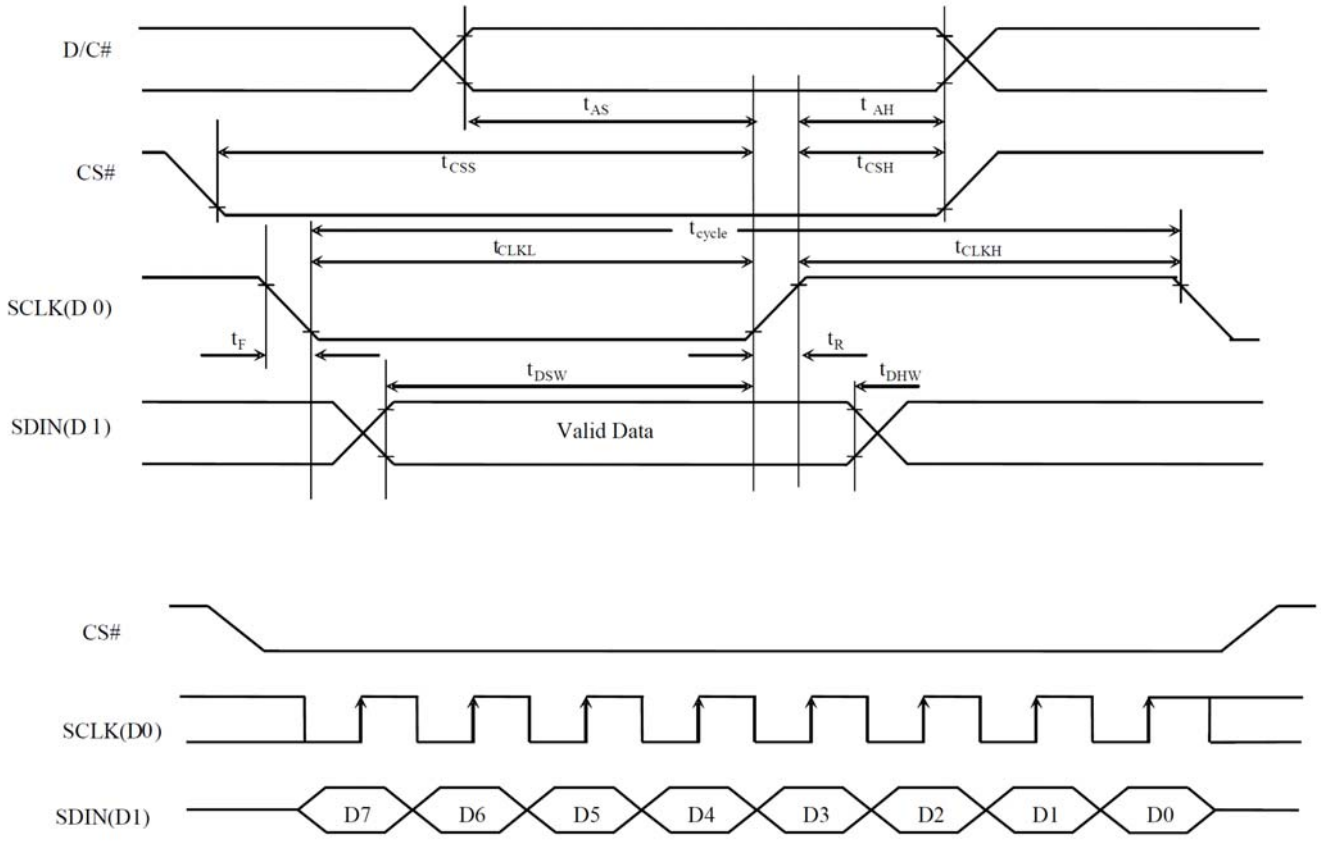


Figure 10-4-4: Serial interface characteristics

(V_{CI} - VSS = 2.4V to 3.3V, T_{OPR} = 25°C, CL=20pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~80%]	-	-	15	ns

Table 10-4-4: Serial Interface Timing Characteristics

11 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

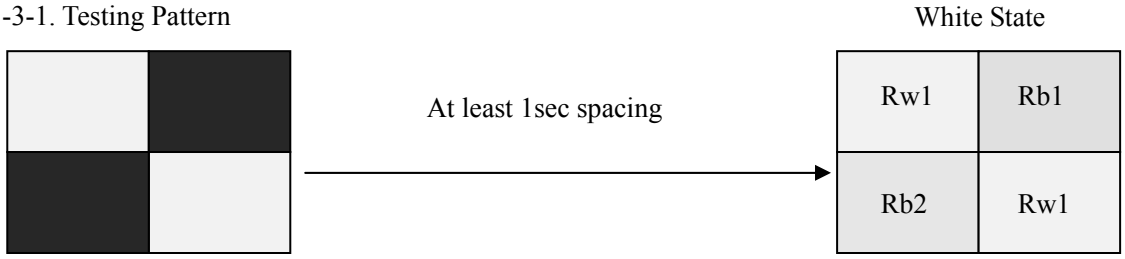
Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	11-1
CR	Contrast Ratio		7:1	8:1	-	-	11-2
T_{update}	Image update time	at 25 °C	-	1800	-	ms	-
Ghosting	Image sticking		-2.0	1.0	2.0	-	11-3

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

11-3. Ghosting Testing:

11-3-1. Testing Pattern



11-3-2. Refresh process：Init ---- GC White ---- 4 checkerboard Pattern GC ---- GC White.

11-3-3. Measuring the reflectance of all 4 checkerboard areas when final white state by Eye-one device.

11-3-4. Rw: reflectance of area transited from white state

Rb: reflectance of area transited from dark(black) state

11-3-5. Calculating averages of WS-to-WS and DS-to-WS transitions:

Rw(ave)=(Rw1+Rw2)/2，Rb(ave)=(Rb1+Rb2)/2，G=Rw(ave)-Rb(ave).

12 Appearance Inspection Standard

12.1 Major Defects

Defect Type	Description
No display	Not able to display any image
Line defect	Complete line(s) missing or unusual appear when display
Abnormal display	Unusual pattern or function when display

12.2 Minor Defects

<table>
<tr><td colspan="2" rowspan="2">Environmental condition</td><td>Temperature / Humidity</td><td>Environmental iliumination</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>20°C -25°C
40%RH-55%RH</td><td>700-1000Lux</td><td>200-300mm</td><td>20 sec</td><td>Up/down 30 degree (Rotation)</td></tr>
<tr><td rowspan="9">appearance Inspection standard</td><td>NO.</td><td>Defect type</td><td>Check</td><td>Acceptable</td><td>A Zone</td><td>B Zone</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">Spot (B/W spot, dent in glass or protection sheet , foreign mat. Swell. Dot defect) (unwork)</td><td rowspan="3">By eye and gauge</td><td>D≦0.2mm</td><td>Ignore</td><td rowspan="7">OK</td></tr>
<tr><td>0.2mm<D≦0.3mm</td><td>≦4（two spot spacing greater than 20mm）</td></tr>
<tr><td>0.3mm<D≦0.35mm</td><td>N≦1</td></tr>
<tr><td rowspan="3">2</td><td rowspan="3">Scratch or line defect (scratch or foreign mat. Protection sheet) (unwork)</td><td rowspan="3">By eye and gauge</td><td>D>0.35mm</td><td>NG</td></tr>
<tr><td>L≦0.5mm & W≦0.2mm</td><td>Ignore</td></tr>
<tr><td>0.5 mm< L≦ 3mm
& 0.2mm<W≦0.3mm</td><td>≦2（the center of two line spacing greater than 30mm）</td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">Air bubble</td><td rowspan="3">By eye and gauge</td><td>L>3.0mm or W>0.3mm</td><td>NG</td></tr>
<tr><td>D1/D2≦0.2mm</td><td>Ignore</td></tr>
<tr><td>0.2mm<D1/D2≦0.5mm</td><td>N≦3</td></tr>
<tr><td>4</td><td>Stab</td><td>By eye</td><td>D1/D2>0.5mm
No hurt PET</td><td>NG
NG</td></tr>
</table>

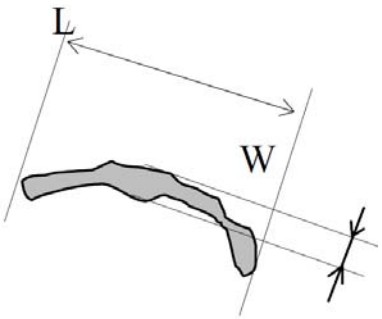
Note: 1. Spot size is based on microscope 10x~100x

2. Spot define: That only can be seen under WS, BS or GS defects.

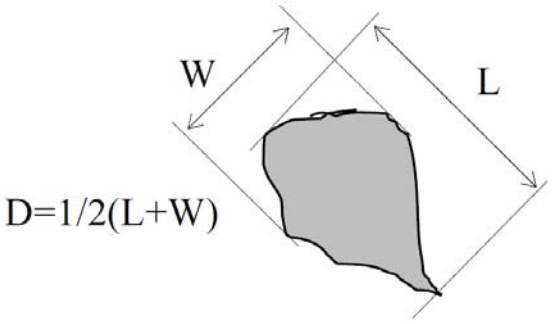
3. A Zone: Active area(defined in specification)

B Zone: Border area from A Zone edge

12.3 Spot and Line Defect Test and Calculation



Spot defect



Line defect

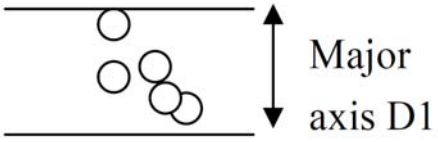
12.4 Spot and Line Test Standard

When L≦0.5mm, test as point.

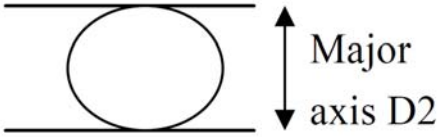
When L< 4W, test as point.

12.5 Air Bubble Defect Test and Calculation

Aggregate of small air



Big air bubble



13 Handling, Safety, and Environment Requirements

Warning
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.
Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

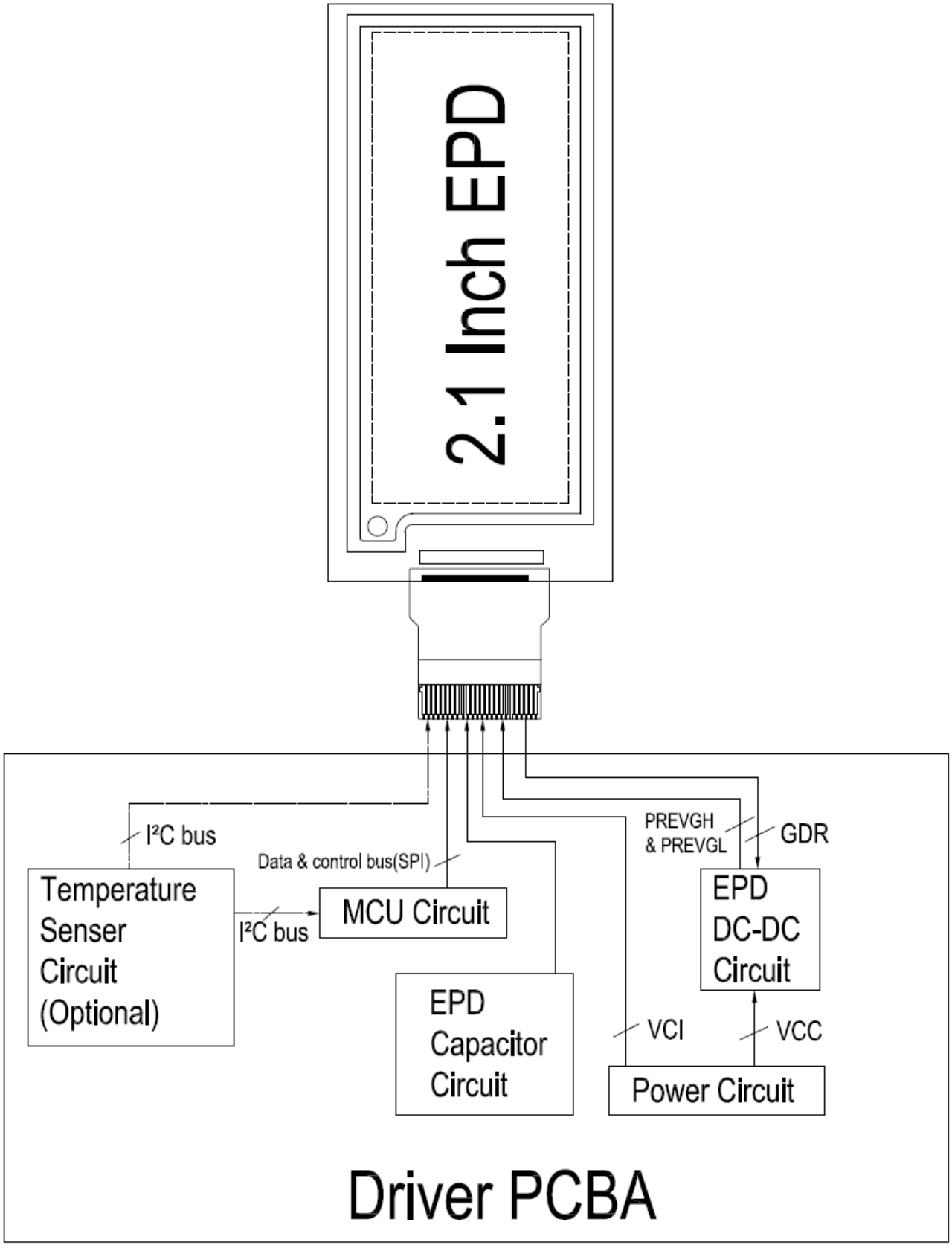
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricality and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

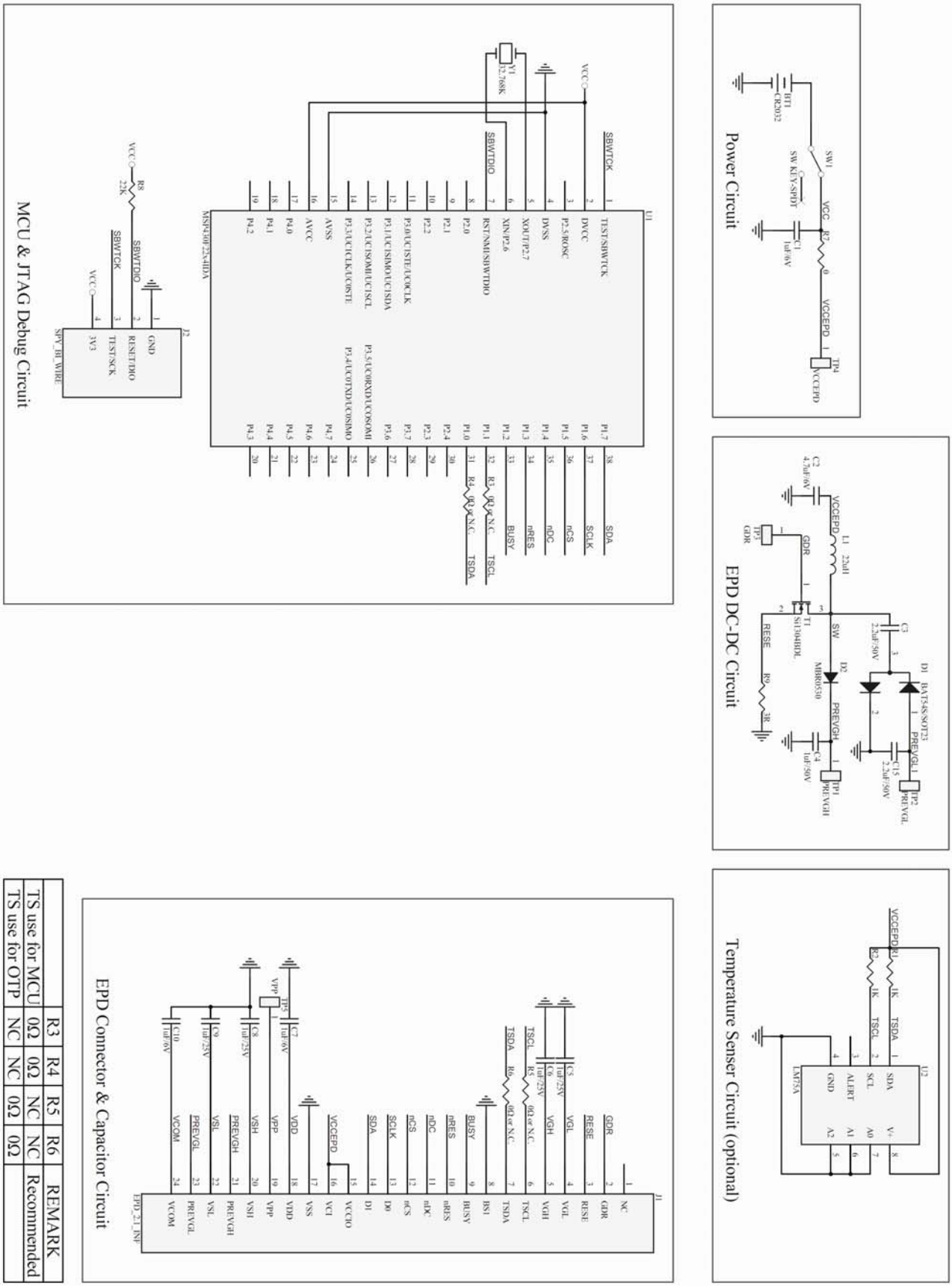
14 Reliability Test

No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 240hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 30 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
11	Altitude test Operation	700hPa (= 3000m) 48Hr		At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
12	Altitude test Storage	260hPa (= 10000m) 48Hr		At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

15 Block Diagram



16 Typical Application Circuit with SPI Interface



	R3	R4	R5	R6	REMARK
TS use for MCU	0Ω	0Ω	NC	NC	Recommended
TS use for OTP	NC	NC	0Ω	0Ω	

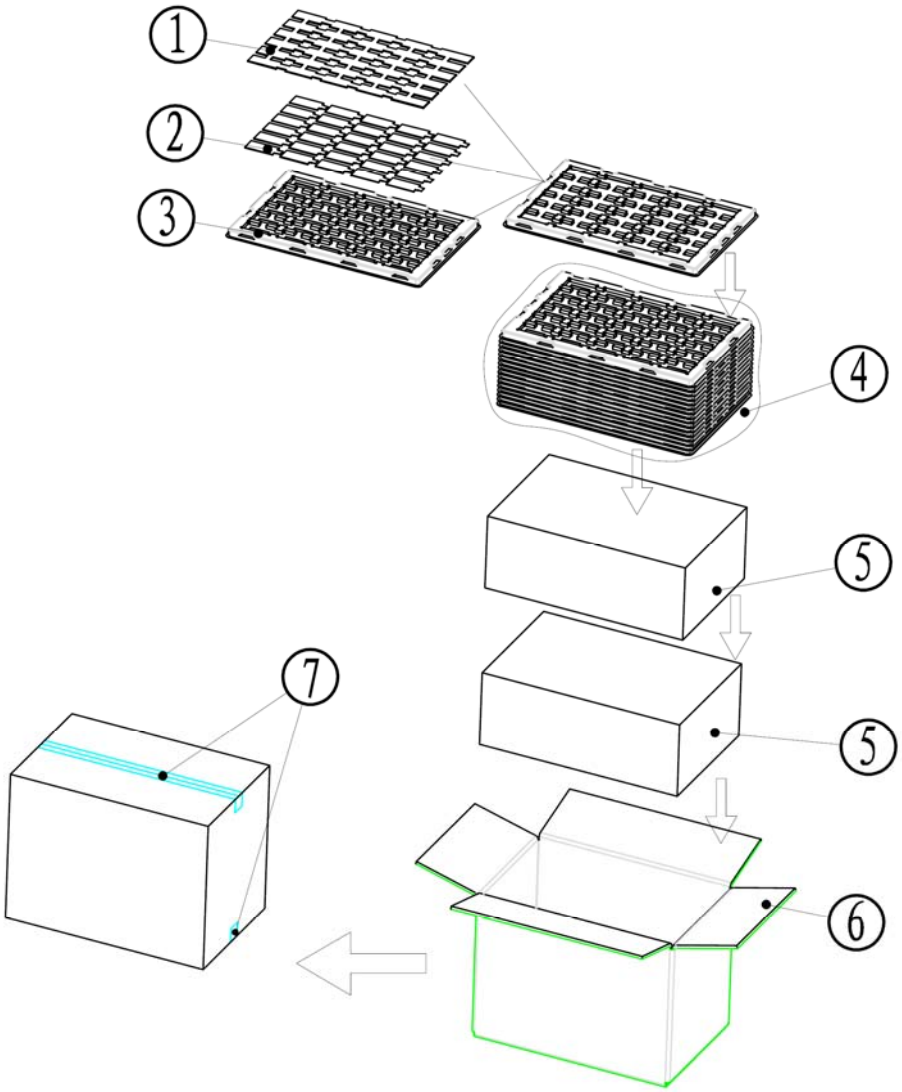
17 Packaging

Packing Form

a) Package quantity in one outer box(2 inner boxes): 840 pcs

b) box size: 458 mm X 303 mm X 310 mm

c) 1 inner box = 14 (full tray) + 1 (dummy / top tray)



No.	Description	Material
①	PE Foam	EPE
②	Board Ass'y (840 pcs/1 Box)	EPD Panel
③	Packing, tray (15 pcs/1 inner box)	PET
④	PE BAG	PE
⑤	inner carton	A3A
⑥	Outer carton	A=A
⑦	Tape (43mm*300m)	OPP